AMENDMENTS TO THE CLAIMS:

The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-9 (Canceled)

Claim 10 (New): A clock generator comprising:

a first detector receiving an input signal and an output oscillating clock, detecting a phase difference between the input signal and the output oscillating clock;

a charge pump, coupled to the first detector, for generating a control signal according to the phase difference; and

a voltage-controlled oscillator (VCO), coupled to the charge pump, for generating the output oscillating clock according to the control signal, wherein the VCO comprising:

a plurality of series-coupled voltage control delay lines (VCDL) for outputting a plurality of oscillating signals respectively to the control signal;

a multiplexer, coupled to the VCDLs, for selecting one of the oscillating signals to be the output oscillating clock according to a second control signal;

a second detector, coupled to the multiplexer, for outputting a detecting signal according to the output oscillating clock and a predetermined frequency; and

a controller, coupled between the multiplexer and the second detector, for determining the second control signal according to the detecting signal.

Claim 11 (New): The clock generator of claim 10, wherein the multiplexer, the second detector, and the controller form a first loop.

Claim 12 (New): The clock generator of claim 11, wherein the first loop is located in

the VCO.

Claim 13 (New): The clock generator of claim 11, wherein the first detector, the charge pump, and the VCO form a second loop.

Claim 14 (New): The clock generator of claim 13, further comprising:

a frequency divider, coupled between the VCO and the first detector, for dividing a frequency of the output oscillating clock, wherein the frequency divider is located in the second loop.

Claim 15 (New): The clock generator of claim 13, further comprising:

a loop filter, coupled between the VCO and the charge pump, for filtering the control signal, wherein the loop filter is located in the second loop.

Claim 16 (New): The clock generator of claim 13, wherein the first detector is only located in the second loop.

Claim 17 (New): The clock generator of claim 11, wherein the second detector is only located in the first loop.

Claim 18 (New): A method for adjusting a frequency of an output oscillating clock, the method comprising:

using a first detector to receive an input signal and the output oscillating clock and detect a phase difference between an input signal and the output oscillating clock;

using a first circuit to generate a control signal according to the phase difference;

using a voltage-controlled oscillator (VCO) to generate a plurality of oscillating signals according to the control signal;

using a multiplexer to select one of the oscillating signals to be the output oscillating clock according to a second control signal;

using a second detector to compare the output oscillating clock and a predetermined frequency and thereby generate a comparison signal; and

using a controller to determine the second control signal according to the comparison signal.

Claim 19 (New): The method of claim 18, wherein the multiplexer, the second

detector, and the controller form a first loop.

Claim 20 (New): The method of claim 19, wherein the first loop is located in the VCO.

Claim 21 (New): The method of claim 19, wherein the first detector, the first circuit, and the VCO form a second loop.

Claim 22 (New): The method of claim 21, further comprising:

using a frequency divider to divide a frequency of the output oscillating clock, wherein the frequency divider is located in the second loop.

Claim 23 (New): The method of claim 21, further comprising:

using a loop filter to filter the control signal, wherein the loop filter is located in the second loop.

Claim 24 (New): The method of claim 21, wherein the first detector is only located in the second loop.

Claim 25 (New): The method of claim 19, wherein the second detector is only located in the first loop.